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AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A magnetic non-volatile memory device provided with a magnetic shielding structure for suppressing the influence of external magnetic fields,

wherein said magnetic non-volatile memory comprises a tunnel-magneto-resistance element, a word line, a bit line, and a selection transistor, the selection transistor being formed at least partially in a silicon substrate,

~~wherein a magnetic shield layer made from a soft magnetic metal is formed at a top and a bottom region of said device for suppressing penetration of magnetic flux into said device,~~

~~wherein said magnetic shield layers are formed at the mounting side of said device, and on a device surface opposite to said mounting side of said device, and~~

wherein a first magnetic shield layer made from a soft magnetic metal is formed over the silicon substrate and a second magnetic shield layer made from a soft magnetic metal is formed over the bit line of the magnetic non-volatile memory, and

wherein said device includes a plurality of layers between the magnetic shield layers, at least one of said plurality of layers and at least one of said magnetic shield layers ~~having~~ being comprised of a same material.

2. (Cancelled)

3. (Currently Amended) The magnetic non-volatile memory device according to claim 1, ~~said device~~ wherein:

each of said first and second magnetic shield ~~layer~~ layers is formed of a nano granular structure having a magnetic layer and a non-magnetic layer.

4. – 6. (Canceled)

7. (Currently Amended) The magnetic non-volatile memory device according to claim [[4]] 1, ~~said device~~ wherein:

said ~~composing element~~ same material includes one selected from the group consisting of Fe, Co, Pt, Mn, and Al.

8. (Currently Amended) A method for manufacturing a magnetic non-volatile memory device provided with a magnetic shielding structure for suppressing the influence of external magnetic fields, said method comprising the steps of:

~~forming a layer of said device and a magnetic shield layer for suppressing penetration of magnetic flux into said device in a single sputtering chamber; and~~

providing said magnetic non-volatile memory comprising a tunnel-magneto-resistance element, a word line, a bit line, and a selection transistor, the selection transistor being formed at least partially in a silicon substrate,

providing a first magnetic shield layer made from a soft magnetic metal over the silicon substrate and a second magnetic shield layer made from a soft magnetic metal over the bit line of the magnetic non-volatile memory, and

wherein ~~using~~ a single target is used for forming at least one of the shield layers and ~~for forming~~ a layer of said magnetic non-volatile memory ~~device~~ located between the magnetic shield layers.

9. (Currently Amended) ~~A~~ An array of magnetic non-volatile memory ~~device~~ devices, each provided with a magnetic shielding structure for suppressing the influence of external magnetic fields,

~~wherein a magnetic shield layer made from a soft magnetic metal is formed at a top and a bottom region of said device for suppressing penetration of magnetic flux into said device,~~

~~wherein said magnetic shield layers are formed at the mounting side of said device, and on a device surface opposite to said mounting side of said device,~~

~~wherein said device includes a plurality of layers between the magnetic shield layers, at least one of said plurality of layers and at least one of said magnetic shield layers having a same material; and~~

wherein each of said magnetic non-volatile memory devices comprises a tunnel-magneto-resistance element, a word line, a bit line, and a selection transistor, the selection transistor being formed at least partially in a silicon substrate,

wherein a first magnetic shield layer made from a soft magnetic metal is formed over the silicon substrate of each of the magnetic non-volatile memory devices and a second magnetic shield layer made from a soft magnetic metal is formed over the bit line of each of the magnetic non-volatile memory devices, and

wherein ~~a plurality of said non-volatile memory devices are arranged in an array and~~ at least one of said magnetic shield layers extends across substantially the

entire array of memory devices.

10. (Currently Amended) ~~A~~ The magnetic non-volatile memory device as defined in claim 9, wherein at least one of said first and second magnetic shield ~~layer~~ layers is formed of a nano-granular structure having a magnetic and a non-magnetic layer.

11. (Canceled)

12. (Currently Amended) A wafer substrate ~~including a plurality of magnetic non-volatile memory devices said wafer~~ comprising:

a plurality of information storage sections attached to a substrate, each said information storage section including a plurality of layers;

a first magnetic shield layer for suppressing the influence of external magnetic fields, said first magnetic shield layer formed across substantially the entire wafer substrate; and

a second magnetic shield layer for suppressing the influence of external magnetic fields, said second magnetic shield layer formed at a side of said plurality of information storage sections opposite said wafer substrate; ~~and~~

wherein each of said information storage sections comprises a tunnel-magneto-resistance element, a word line, a bit line, and a selection transistor, the selection transistor being formed at least partially in the wafer substrate,

wherein the first magnetic shield layer is formed over the substrate of each of the information storage sections in which the selection transistor is at least partially

formed, and the second magnetic shield layer is formed over the bit line of each of the information storage sections,

wherein at least one of said plurality of layers of said information storage sections and at least one of said magnetic shield layers ~~have~~ are comprised of a same material.

13. (Canceled)

Please add the following new claims:

14. (New) The magnetic non-volatile memory device according to claim 1, wherein said second magnetic shield layer is formed on the bit line, and said first magnetic shield layer is formed on a surface of the silicon substrate opposite the surface of the silicon substrate in which the selection transistor is formed.

15. (New) The method for manufacturing a magnetic non-volatile memory device according to claim 8, wherein said second magnetic shield layer is provided on the bit line, and said first magnetic shield layer is provided on a surface of the silicon substrate opposite the surface of the silicon substrate in which the selection transistor is formed.

16. (New) The array of magnetic non-volatile memory devices according to claim 9, wherein said second magnetic shield layer is formed on the bit line of each of the magnetic non-volatile memory devices, and said first magnetic shield layer is formed on a surface of the silicon substrate of each of the magnetic non-volatile

memory devices opposite the surface of the silicon substrate in which the selection transistor is formed.

17. (New) The magnetic non-volatile memory device according to claim 1, further comprising a third magnetic shield layer formed on a side surface of the magnetic non-volatile memory such that the third shield layer interfaces with at least a portion of both the first and the second magnetic shield layers and such that all three shield layers are magnetically coupled.

18. (New) The method for manufacturing a magnetic non-volatile memory device according to claim 8, further comprising a step of providing a third magnetic shield layer formed on a side surface of the magnetic non-volatile memory such that the third shield layer interfaces with at least a portion of both the first and the second magnetic shield layers and such that all three shield layers are magnetically coupled.

19. (New) The array of magnetic non-volatile memory devices according to claim 9, further wherein a third magnetic shield layer is formed on a side surface of each of the magnetic non-volatile memory devices such that the third shield layer interfaces with at least a portion of both the first and the second magnetic shield layers of each of the respective magnetic non-volatile memory devices and such that all three shield layers are magnetically coupled.

20. (New) The magnetic non-volatile memory device according to claim 1, wherein said bit line is electrically connected to said tunnel-magneto-resistance element.

21. (New) The method for manufacturing a magnetic non-volatile memory device according to claim 8, wherein said bit line is electrically connected to said tunnel-magneto-resistance element.

22. (New) The array of magnetic non-volatile memory devices according to claim 9, wherein said bit line of each respective magnetic non-volatile memory device is electrically connected to the tunnel-magneto-resistance element of the same respective magnetic non-volatile memory device.

23. (New) The magnetic non-volatile memory device according to claim 1, further comprising an electrical insulating barrier layer formed between the bit line and the second magnetic shield layer.

24. (New) The method for manufacturing a magnetic non-volatile memory device according to claim 8, further comprising the step of providing an electrical insulating barrier layer between the bit line and the second magnetic shield layer.

25. (New) The array of magnetic non-volatile memory devices according to claim 9, wherein each respective magnetic non-volatile memory device includes an electrical insulating barrier layer formed between the bit line and the second magnetic shield layer.